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NOV 14 2005

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	10/619,798
Filing Date	July 17, 2003
First Named Inventor	Subir Ghosh
Group Art Unit	2188
Examiner Name	Kevin L. Ellis

Sheet	1	of	2	Attorney Docket Number	OPTI 3140-6

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
UK	A1	5,353,415		Wolford et al.	10-04-1994	
	A2	5,420,991		Konigsfeld et al.	05-30-1995	
	A3	5,511,226		Zilka	04-23-1996	
	A4	5,572,702		Sarangdhar et al.	11-05-1996	
	A5	5,335,335		Jackson et al.	08-02-1994	
	A6	5,072,369		Theus et al.	12-10-1991	
NK	A7	5,325,503		Stevens et al.	06-28-1994	
	A8					
	A9					
	A10					
	A11					
	A12					
	A13					
	A14					
	A15					
	A16					
	A17					
	A18					
	A19					
	A20					

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
HK	B1		EP 0 288 649		Gach et al.	11-02-1988		
HN	B2		EP 0 261 029		Rubinfeld	09-15-1987		
	B3							
	B4							
	B5							
	B6							
	B7							
	B8							
	B9							
	B10							

Examiner Signature	*Kevin L. Ellis*	Date Considered	4/18/06

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[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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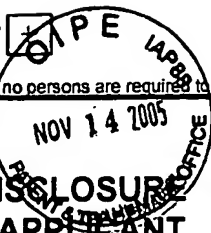
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Sheet	2	of 2	Attorney Docket Number	OPTI 3140-6

		OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
UK	C1	TOM SHANLEY and DON ANDERSON, Rev2, "PCI System Architecture", PC System Architecture Series, Vol. 4, Version 2, Second Edition 1993, published by MindShare Inc., Chapter 16.	
UK	C2	TOM SHANLEY and DON ANDERSON, Rev3, "PCI System Architecture" PC System Architecture Series, Third Edition 1995, published by MindShare Inc., Chapter 21	

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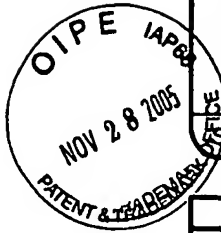
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	Group Art Unit	2188
	Examiner Name	ELLIS, Kevin L.
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𝓊𝓚	C1	MOTOROLA INC., "PowerPC 601 RISC Microprocessor Technical Summary", Freescale Semiconductor, Inc., 1993	
𝓊𝓚	C2	NORMAN P. JOUPPI, "Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, 18 Computer Architecture News 364-373, 1990	
𝓊𝓚	C3	NORMAL P. JOUPPI, "Reducing Compulsory and Capacity Misses", WRL Technical Note TN-53, August 1990	
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𝒰𝓚	C7	ALAN JAY SMITH, "Cache Memories", 14 ACM Computing Surveys 473-530, 1982	
𝒲𝓡	C8	JEAN-LOUP BAER & TIEN-FU CHEN, "An Effective On-Chip Preloading Scheme to Reduce Data Access Penalty", In Proceedings of Supercomputing '91 at 176-86, 1991	
𝒲𝓚	C9	TIEN-FU CHEN & JEAN-LOUP BAER, "Effective Hardware-Based Data Prefetching for High Performance Processors, 44 IEEE Transactions on Computer 609-623, May 1995	
𝓊𝓚	C10	TIEN-FU CHEN & JEAN-LOUP BAER, "A Performance Study of Software and Hardware Prefetching", 22 Computer Architecture News 223-232, 1994	
𝒲𝓚	C11	TIEN-FU CHEN & JEAN-LOUP BAER, "Reducing Memory Latency via Non-blocking and Prefetching Caches", Fifth International Conference on Architectural Support for Programming Languages and Operating Systems at 51-61, 1992	

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ᴗᴕ	C12	LUCIEN CENSIER & PAUL FEAUTRIER, "A New Solution to Coherence Problems in Multicache Systems", 27 IEEE Transactions on Computers 1112-1118, 1978	
ᴗᴕ	C13	MICHEL DUBOIS ET AL., "Memory Access Buffering in Multiprocessors", 14 Computer Architecture News 434-442, 1986	
ᴗᴕ	C14	JOHN W.C. FU & JANAK H. PATEL, "Data Prefetching in Multiprocessor Vector Cache Memories", Proceedings of the 18th Annual International Symposium on Computer Architecture at 54-63, 1991	
ᴗᴕ	C15	JOHN W.C. FU & JANAK H. PATEL, "Stride Directed Prefetching in Scalar Processors", Proceedings of the 25th Annual International Symposium on Microarchitecture at 102-10, 1992	
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ᴗᴕ	C18	DAVID KROFT, "Lockup-Free Instruction Fetch-Prefetch Cache Organization", Proceedings of the 8th Annual International Symposium on Computer Architecture at 81-5, 1981	
ᴗᴕ	C19	ROLAND L. LEE, "The Effectiveness of Caches and Data Prefetch Buffers in Large-Scale Shared Memory Multiprocessors", (May 1987) (Ph.D. thesis, University of Illinois at Urbana-Champaign)	
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ᴗᴕ	C22	ALLAN K. PORTERFIELD, "Software Methods for Improvement of Cache Performance on Supercomputer Applications (May 1989) (Ph.D. thesis, Rice University)	

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WK	C23	TIEN-FU CHEN, "Data Prefetching for High-Performance Processors (July 1993) (Ph.D. Thesis, University of Washington)	
	C24		

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